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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,275	JANZEN, JEFFERY W.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The eleven information disclosure statement (IDS) submitted on 8 April 2004, 8 June 2004, 18 August 2004, 22 November 2004, 18 January 2005, 25 April 2005, 27 June 2005, 26 July 2005, 29 August 2005, 13 February 21006, and 1 May 2006 were fully considered by the Examiner.

Drawings

2. The drawings received on 8 April 2004 are objected to because Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because of the following:

The extraneous markings located on the abstract should be removed (i.e. "H:\IP\...filed.doc").

Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1-25, and 27-28 are objected to because of the following informalities:

As for claims 1, the phrases "adjacent a first end" and "adjacent a second end" (lines 6 and 7 of the claim respectively) should be changed to "adjacent with a first end", and "adjacent with a second end" for clarity. Similar objections with respect to changing the phrase "adjacent" to "adjacent with" are applicable to claims 5, 7, 9, 10, 14, 16, 18, 20, 21, 25, and 27.

As for claims 3, 12, and 22, acronyms such as DRAM, should not be written in abbreviated form unless they have been previously set forth within the claims expanded form. An acceptable alternative includes "Dynamic Read Only Memory (DRAM)".

As for claim 21, the word "lease" as recited in line 7 of the claim should be changed to "least".

Claims 2, 4, 5, 6, 8, 9, 11, 13, 15, 17, 19, 23-24, and 28 are objected to for further limiting one of the claims previously objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 1, 10, 21 and 26, the phrase "approximately a center of the circuit board" (line 3 of claim 1 for example) renders the claims indefinite, as one of ordinary skill in the art would be unable to determine the metes and bounds of this limitation. Furthermore, the specification fails to provide any standard for ascertaining the requisite degree to which the term "approximately" limits the scope of the invention. The clams will further be treated on their merits based on the assumption that "approximately a center of the circuit board" was intended to mean the true center of the circuit board.

As for claim 29, the phrase "substantially parallel edges of the circuit board" (lines 2-3 of the claim) renders the claims indefinite, as one of ordinary skill in the art would be unable to determine the metes and bounds of this limitation. Furthermore, the specification fails to provide any standard for ascertaining the requisite degree to which the term "substantially parallel" limits the scope of the invention. The clams will further be treated on their merits based on the assumption that the signal lines recited in this claim are in fact "parallel [to the] edges of the circuit board".

As for claim 26, the phrase "rotated 180 degrees relative to the other device in the pair" renders the claim indefinite as it is unclear which axis said rotation occurs about. Does the recited rotation occur about a vertical (z-axis in

three dimensional Cartesian space) axis of the device itself, or about a vertical or horizontal axis with respect to the hub itself? The Examiner assumes the former for the purposes of applying art.

Claim 1 recites the limitation "the device" in lines 6 and 7 of the claim. There is insufficient antecedent basis for this limitation in the claim, as a plurality of memory devices are previously set forth in the claim. Which device is "the device" referring to in each of the recitations? Additionally the claim recites "the first ends" (line 7 of the claim), however only one first end is previously set forth in this claim. Similar rejections apply to claims 10, 21 and 26.

Claim 6 recites the limitation "the data bus" in line 1 of this claim. There is insufficient antecedent basis for this limitation in the claim as a data bus is not previously set forth within this claim, or the claim from which it depends. A similar rejection applies to claims 15 and 17.

Claim 8 recites the limitation "the data busses" in line 1 of this claim. There is insufficient antecedent basis for this limitation in the claim as data busses are not previously set forth within this claim, or the claim from which it depends. A similar rejection applies to claim 19.

The remaining claims are rejected for further limiting a previously rejected claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5-12, and 14-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nuxoll et al. (US Patent 6,490,188 B2), hereinafter Nuxoll, and in further view of Ryan (US PG Publication 2004/0044833 A1).

As for claims 1, 10, and 21, Nuxoll teaches a memory module comprising:

a data input device (Fig. 5 (654));

a data output device (Fig. 5 (656));

a processor coupled to the data input and data output devices (Fig. 5 (652));

memory modules comprising:

a circuit board (Fig. 3a (31));

a plurality of memory devices arranged in pairs (Fig. 3a (33 and 35)), each memory device including pins associated with a first functional group of signals adjacent a first end of the device and pins associated with a second functional group of signals adjacent a second end of the device (referring to table 4 (col. 14, lines 40-63), the pin out of each memory module (as depicted in the Fig. 4) comprises a first functional group of pins (i.e. data pins) on the left side of the memory (i.e. pins 101-103 are a data (DQ) group of pins) and a second functional group of pins (i.e. control-address pins) on the right side of the memory (i.e. pins 149-152 are RQ, CTM, and CTMN pins used for control and addressing of the memory)), and the first ends of the devices in each pair being positioned

adjacent one another on the circuit board and the second end of each device in a pair being positioned adjacent a second end of a device in one of the other pairs (referring to Fig. 3A – mirrored pairs of memory modules are repeated (i.e. device 35 mirrors device 33 such that a first side of each mirrored pair is adjacent to each other, and a second side of a pair is adjacent to a second side of a pair adjacent a first pair – col. 10, line 60 through col. 11, line 9)); and

an edge connector positioned along an edge of the circuit board (Fig. 3a (32)).

Despite these teachings, Nuxoll fails to teach the plurality of devices as being arranged around a centrally positioned memory hub coupled to the edge connector as claimed by Applicant. Additionally, Nuxoll fails to teach a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link.

Ryan however teaches a system and method for optimizing interconnections of memory devices in a multichip module in which a plurality of memory devices (212, 214, etc.) are arranged around a centrally located memory hub (208) – Fig. 2. Also note the memory devices communicate with external devices (i.e. a controller (200)) via an external memory line (203) – paragraphs 0018 through 0019, all lines. Ryan additionally teaches a controller (Fig. 2 (200) being operable to receive and transmit memory signals on a high-speed data link (paragraph 0019, all lines)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nuxoll to further include Ryan's system and method for optimizing

interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Nuxoll would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

As for claim 26, Nuxoll teaches a method of forming a memory module including a circuit board, the method comprising:

positioning a plurality of memory devices in a respective pair being physically rotated 180 degrees relative to the other device in the pair (referring to Fig. 3a, each pair (33, 35) is physically rotated 180 degrees in order to perform a side-by-side mirroring of the pair (col. 7, line 66 through col. 8, line 21));

Despite these teachings, Nuxoll fails to teach the plurality of devices as being arranged around a centrally positioned memory hub coupled to the edge connector. Furthermore, Nuxoll teaches to specifically teach coupling data and control-address signals between the memory devices and the hub, and routing a system bus to the memory hub as claimed by Applicant.

Ryan however teaches a system and method for optimizing interconnections of memory devices in a multichip module in which a plurality of memory devices (212, 214, etc.) are arranged around a centrally located memory hub (208) – Fig. 2. Also note the memory devices communicate with an external devices (i.e. a controller (200)) via external memory line (203) – paragraphs 0018 through 0019, all lines. Ryan additionally teaches a controller (Fig. 2 (200) being operable to receive and transmit

memory signals on a high-speed data link (paragraph 0019, all lines)). The busses supply address-control and data signals to and from the memory devices.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nuxoll to further include Ryan's system and method for optimizing interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Nuxoll would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

As for claims 2, and 11, Nuxoll teaches a memory module wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals (referring to table 4 (col. 14, lines 40-63), the pin out of each memory module (as depicted in the Fig. 4) comprises a first functional group of pins (i.e. data pins) on the left side of the memory (i.e. pins 101-103 are a data (DQ) group of pins) and a second functional group of pins (i.e. control-address pins) on the right side of the memory (i.e. pins 149-152 are RQ, CTM, and CTMN pins used for control and addressing of the memory)).

As for claims 3, 12, and 22, Nuxoll teaches the memory module of claim 1 wherein the memory devices comprise DRAMs (Nuxoll teaches the memory devices as being DRAM type devices – col. 6, lines 49-66).

As for claim 27, Nuxoll teaches the method of claim 26 wherein each memory device includes a pin 1 designated end and a first functional group of signals are

adjacent this end of the device, and wherein the devices in each pair are positioned with the pin 1 designated ends adjacent one another (referring to Fig. 3a, each pair of memory devices are mirrored side-by-side such that pin 1 of each memory device within a pair are adjacent to one another).

As for claim 28, Nuxoll teaches the method of claim 27 wherein the first functional group of signals comprises data bus signals (as per the rejection of claim 2).

As for claims 5, and 14, though Nuxoll teaches the first functional group of signals comprising data signals and the second functional group of signals comprising control-address signals (as per the rejection of claim 2), he fails to teach the module as including four pairs of devices, each pair being positioned adjacent to a respective edge of the circuit board.

Ryan however teaches a system and method for optimizing interconnections of memory devices in a multichip module in which 4 pairs of memory devices (212, 214, etc.) are each arranged around a respective edge of a the circuit board – Fig. 2

As for claims 6, and 15, Nuxoll teaches the memory module of claim 5 wherein the data bus of each memory device is 9-bits wide (9 DQ bits are sent across the bus as one byte of data (DQ0-DQ8)) – col. 12, lines 1-6.

As for claims 7, and 18, Nuxoll (in further view of Ryan) teaches the memory module of claim 1, wherein the module includes eight pairs of memory devices, four pairs positioned on a front side of the circuit board and four pairs positioned on a back side of the circuit board (totaling 8), each pair on the front side being positioned adjacent a corresponding pair on the back side, and wherein the eight pairs of memory

devices comprise a single rank on the memory module (as discussed in claim 5, Ryan teaches four pairs of memory devices. Additionally, Nuxoll teaches that mirroring memory devices on both the front and back side of the circuit board is well known in the art (col. 2, lines 17-41)).

As for claims 8 and 19, Nuxoll teaches the memory module of claim 7, wherein the data busses of half the memory devices are 4-bits wide and the data busses of the other half of memory devices are 5 bits wide (as discussed in claim 5, Nuxoll teaches the memory bus as comprising a total of 9-bits). Though Nuxoll does not explicitly teach half of the memory devices as being 4-bits wide, and the other half being 5-bits wide, such a limitation is merely a matter of design choice and would have been obvious in the system of Nuxoll. The limitation of splitting the 9-bit wide memory bus into a first half comprising 4-bits, and the other half 5-bits fails to define a patentably distinct invention over Nuxoll, since both the instant invention as a whole and Noxoll's teachings are directed to mirroring the pin configuration of pairs of memory devices.

As for claims 9, 20, and 25, Nuxoll teaches the memory module of claim 1, wherein the plurality of memory devices positioned around the memory hub are positioned on a front side of the circuit board, and wherein the memory module further comprises a second rank of memory devices positioned on a back side of the circuit board, each device on the back side being positioned adjacent a corresponding device on the front side (as discussed in claim 5, Ryan teaches four pairs of memory devices. Additionally, Nuxoll teaches that mirroring memory devices on both the front and back side of the circuit board is well known in the art (col. 2, lines 17-41)).

As for claim 16, Ryan teaches the memory module of claim 10 wherein the module includes a first pair of memory devices positioned adjacent a respective edge of the circuit board and a second pair positioned adjacent an opposite edge of the circuit board (Fig. 2., each memory pair (i.e. 212, 214) is arranged adjacent a pair located on a second edge of the board (i.e. 222, 220). Note, Though Ryan does not explicitly teach pairs of memory devices as being opposite on a diagonal from each other (rather they are opposite with respect to a horizontal and/or vertical axis), such a limitation is merely a matter of design choice and would have been obvious in the system of Ryan. The mere positioning of opposite pairs (either being opposites with respect to a horizontal or diagonal axis of the board) fails to define a patentably distinct invention over Ryan since both the instant invention as a whole and Ryan's teachings are directed minimizing propagation delay between separate pairs of memory devices. The difference in propagation delay between each set of opposite pairs would be equal regardless of their position on the board (i.e. opposites with respect to a horizontal or diagonal axis)).

As for claim 17, though Nuxoll teaches the memory module of claim 16 wherein the data bus of each memory device is 9-bits wide (as per the rejection of claim 6), he fails to teach the memory bus as being 18-bits wide. Such a limitation however is merely a matter of design choice and would have been obvious in the system of Nuxoll. The limitation an using an 18-bit wide memory bus (rather than a 9-bit as expressly taught by Nuxoll) fails to define a patentably distinct invention over Nuxoll, since both the instant invention as a whole and Noxoll's teachings are directed mirroring the pin configuration of pairs of memory devices.

As for claim 23, Ryan teaches the computer system of claim 21 wherein the memory modules are coupled in a daisy chain manner to the controller (referring to Fig. 4, each memory module (201, 302) is connected to the controller (not shown in this figure, but shown in Fig. 2 (200), in a daisy chained fashion via a connecting bus (401))).

As for claim 24, Ryan teaches the computer system of claim 21 wherein the high-speed data link comprises an optical communications link (paragraph 0019, all lines).

As for claim 29, Ryan teaches the method of claim 26 wherein a data bus is routed between the hub and each device, and wherein signal lines of the data bus are routed substantially parallel edges of the circuit board (referring to Fig. 2, each bus (230, 232) is routed parallel with the edges of the board).

As for claim 30, the Ryan discloses the method of claim 26 wherein a control-address bus is routed between the hub and one device in each pair (Fig. 2, each bus is routed to one device. The bus contains control and data signals), and wherein signal lines of the control-address bus as being routed diagonally outward from the hub towards corners of the circuit board (though Ryan does not explicitly teach signal lines of the control-address bus are routed diagonally outward from the hub towards corners of the circuit board, such a limitation is merely a matter of design choice and would have been obvious in the system of Ryan. The mere routing of the signal lines (either orthogonally, or diagonally) fails to define a patentably distinct invention over Ryan since both the instant invention as a whole, and Ryan's teachings are directed minimizing propagation delay between separate pairs of memory devices. The

difference in propagation delay between each set of opposite pairs would be equal regardless of the routing position of the signal lines on the board).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nuxoll to further include Ryan's system and method for optimizing interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Nuxoll would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

7. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Nuxoll (US Patent 6,490,188 B2) and Ryan (US PG Publication 2004/0044833 A1), and in further view of D'Antonio et al. (US Patent 6,772,261 B1), hereinafter D'Antonio.

As for claims 4 and 13, Nuxoll teaches the memory module of claim 1, further comprising a second edge connector positioned along a second edge of the circuit board and coupled to the memory hub.

D'Antonio however teaches an interface device that allows testing and using memory modules in computer system not designed for the modules, which includes a module (Fig. 4, 200) comprises both first and second edge connectors (Fig. 4, the board has connector pads on both sides of the board (i.e. (324 and 318) – col. 7, lines 64 through col. 8, line 12)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Nuxoll to further include D'Antonio's memory module interface system into his own system for mirroring memory devices. By doing so, Nuxoll would be able to exploit the benefits of D'Antonio's system which includes an increased flexibility in the interchangeability of various DIMM cards; hence permitting his system to take advantage of utilizing a greater variety of in-line memory modules compatible with his system, as taught by D'Antonio in col. 1, lines 15-35.

Double Patenting

8. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

9. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

10. Claim 1 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of copending Application No. 11/417,389. This is a

provisional double patenting rejection since the conflicting claims have not in fact been patented.

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

12. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

13. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 2-3, 10-12, and 21-22 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 11/417,389 (hereinafter Application '379) in view of Nuxoll (US Patent 6,490,188 B2).

This is a provisional obviousness-type double patenting rejection.

As for claims 10, and 21, Application '379 teaches a memory module comprising:

a circuit board;

a memory hub positioned in approximately a center of the circuit board;

a plurality of memory devices positioned around the memory hub and arranged in pairs, each memory device including pins associated with a first functional group of signals adjacent a first end of the device and pins associated with a second functional group of signals adjacent a second end of the device, and the first ends of the devices in each pair being positioned adjacent one another on the circuit board and the second end of each device in a pair being positioned adjacent a second end of a device in one of the other pairs; and

an edge connector positioned along an edge of the circuit board and coupled to the memory hub.

Application '379 however fails to teach the remaining limitations of these claims.

Nuxoll however teaches:

a data input device (Fig. 5 (654));

a data output device (Fig. 5 (656));

a processor coupled to the data input and data output devices (Fig. 5 (652));

As for claims 3, 12, and 22, Nuxoll teaches the memory module of claim 1 wherein the memory devices comprise DRAMs (Nuxoll teaches the memory devices as being DRAM type devices – col. 6, lines 49-66).

As for claims 2, and 11, Nuxoll teaches a memory module wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals (referring to table 4 (col. 14, lines 40-63), the pin out of each memory module (as depicted in the Fig. 4) comprises a first functional group of pins (i.e. data pins) on the left side of the memory (i.e. pins 101-103 are a data (DQ) group of pins) and a second functional group of pins (i.e. control-address pins) on the right side of the memory (i.e. pins 149-152 are RQ, CTM, and CTMN pins used for control and addressing of the memory)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Noxoll's system for mirroring memory devices. By doing so, Application '379 would be able to exploit the capital savings and process simplification as taught by Nuxoll in col. 4, lines 22-32.

15. Claims 5-9, 14-20, and 23-25 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over the

combined teachings of copending Application '379 and Nuxoll (US Patent 6,490,188 B2), and in further view of Ryan (US PG Publication 2004/0044833 A1).

As for claims 5, and 14, though Application '379 teaches the first functional group of signals comprising data signals and the second functional group of signals comprising control-address signals (as per the rejection of claim 2), it fails to teach the module as including four pairs of devices, each pair being positioned adjacent to a respective edge of the circuit board.

Ryan however teaches a system and method for optimizing interconnections of memory devices in a multichip module in which 4 pairs of memory devices (212, 214, etc.) are each arranged around a respective edge of a the circuit board – Fig. 2

As for claims 6, and 15, Nuxoll teaches the memory module of claim 5 wherein the data bus of each memory device is 9-bits wide (9 DQ bits are sent across the bus as one byte of data (DQ0-DQ8)) – col. 12, lines 1-6.

As for claims 7, and 18, Application '379 (in further view of Ryan) teaches the memory module of claim 1, wherein the module includes eight pairs of memory devices, four pairs positioned on a front side of the circuit board and four pairs positioned on a back side of the circuit board (totaling 8), each pair on the front side being positioned adjacent a corresponding pair on the back side, and wherein the eight pairs of memory devices comprise a single rank on the memory module (as discussed in claim 5, Ryan teaches four pairs of memory devices. Additionally, Nuxoll teaches that mirroring memory devices on both the front and back side of the circuit board is well known in the art (col. 2, lines 17-41)).

As for claims 8 and 19, Application '379 in further view of Nuxoll teach the memory module of claim 7, wherein the data busses of half the memory devices are 4-bits wide and the data busses of the other half of memory devices are 5 bits wide (as discussed in claim 5, Nuxoll teaches the memory bus as comprising a total of 9-bits). Though Nuxoll does not explicitly teach half of the memory devices as being 4-bits wide, and the other half being 5-bits wide, such a limitation is merely a matter of design choice and would have been obvious in the system of Nuxoll. The limitation of splitting the 9-bit wide memory bus into a first half comprising 4-bits, and the other half 5-bits fails to define a patentably distinct invention over Nuxoll, since both the instant invention as a whole and Noxoll's teachings are directed to mirroring the pin configuration of pairs of memory devices.

As for claims 9, and 20, and 25, Application '379 in further view of Nuxoll teaches the memory module of claim 1, wherein the plurality of memory devices positioned around the memory hub are positioned on a front side of the circuit board, and wherein the memory module further comprises a second rank of memory devices positioned on a back side of the circuit board, each device on the back side being positioned adjacent a corresponding device on the front side (as discussed in claim 5, Ryan teaches four pairs of memory devices. Additionally, Nuxoll teaches that mirroring memory devices on both the front and back side of the circuit board is well known in the art (col. 2, lines 17-41)).

As for claim 16, Ryan teaches the memory module of claim 10 wherein the module includes a first pair of memory devices positioned adjacent a respective edge of

the circuit board and a second pair positioned adjacent an opposite edge of the circuit board (Fig. 2., each memory pair (i.e. 212, 214) is arranged adjacent a pair located on a second edge of the board (i.e. 222, 220). Note, Though Ryan does not explicitly teach pairs of memory devices as being opposite on a diagonal from each other (rather they are opposite with respect to a horizontal and/or vertical axis), such a limitation is merely a matter of design choice and would have been obvious in the system of Ryan. The mere positioning of opposite pairs (either being opposites with respect to a horizontal or diagonal axis of the board) fails to define a patentably distinct invention over Ryan since both the instant invention as a whole and Ryan's teachings are directed minimizing propagation delay between separate pairs of memory devices. The difference in propagation delay between each set of opposite pairs would be equal regardless of their position on the board (i.e. opposites with respect to a horizontal or diagonal axis)).

As for claim 17, though Application '379 in further view of Nuxoll teaches the memory module of claim 16 wherein the data bus of each memory device is 9-bits wide (as per the rejection of claim 6), it fails to teach the memory bus as being 18-bits wide. Such a limitation however is merely a matter of design choice and would have been obvious in the system of Nuxoll. The limitation an using an 18-bit wide memory bus (rather than a 9-bit as expressly taught by Nuxoll) fails to define a patentably distinct invention over Nuxoll, since both the instant invention as a whole and Noxoll's teachings are directed mirroring the pin configuration of pairs of memory devices.

As for claim 23, Ryan teaches the computer system of claim 21 wherein the memory modules are coupled in a daisy chain manner to the controller (referring to Fig.

4, each memory module (201, 302) is connected to the controller (not shown in this figure, but shown in Fig. 2 (200), in a daisy chained fashion via a connecting bus (401))).

As for claim 24, Ryan teaches the computer system of claim 21 wherein the high-speed data link comprises an optical communications link (paragraph 0019, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Ryan's system and method for optimizing interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Application '379 would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

16. Claims 4 and 13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over combined teachings of Application '379, Nuxoll (US Patent 6,490,188 B2), and Ryan (US PG Publication 2004/0044833 A1), and in further view of D'Antonio et al. (US Patent 6,772,261 B1), hereinafter D'Antonio.

As for claims 4 and 13, Nuxoll teaches the memory module of claim 1, further comprising a second edge connector positioned along a second edge of the circuit board and coupled to the memory hub.

D'Antonio however teaches an interface device that allows testing and using memory modules in computer system not designed for the modules, which includes a

module (Fig. 4, 200) comprises both first and second edge connectors (Fig. 4, the board has connector pads on both sides of the board (i.e. (324 and 318) – col. 7, lines 64 through col. 8, line 12)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include D'Antonio's memory module interface system into his own system for mirroring memory devices. By doing so, Application '379 would be able to exploit the benefits of D'Antonio's system which includes an increased flexibility in the interchangeability of various DIMM cards; hence permitting his system to take advantage of utilizing a greater variety of in-line memory modules compatible with his system, as taught by D'Antonio in col. 1, lines 15-35.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

7/20/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER